IEEE

SAN FRANCISCO BAY AREA
NANOTECHNOLOGY COUNCIL

February 2008 Seminar

Subject: **Performance Limitations of Cu/low-κ Interconnects and Possible Alternatives**

Speaker: **Professor Krishna Saraswat**
Stanford University, Department of Electrical Engineering

Date: Tuesday, February 19, 2008
Time: Registration & light lunch 11:30am. Presentation & Q/A 12:00 to 1pm

Location: National Semiconductor Bldg E-1 CMA Room. 2900 Semiconductor Drive, Santa Clara, CA
http://www.google.com/search?hl=en&q=2900+Semiconductor+Drive.+santa+clara%2C+ca&btnG=Google+Search
Cost: IEEE Members and Students $5. Non-Members $10

Please RSVP at our web site: www.ieee.org/nano

Talk Abstract:

For more than 30 years, the performance of silicon integrated circuits has improved at an astonishing rate. However, looking into the future the relentless scaling paradigm is threatened by fundamental limits including excessive power dissipation, insufficient communication bandwidth, and signal latency for both off-chip and on-chip application. Many of these obstacles stem from the physical limitation of Cu-based electrical wires, making it imperative to examine alternate interconnect schemes for future This is further exacerbated by the increase in copper resistivity, as wire dimensions and grain size become comparable to the bulk mean free path of electrons in copper (~40nm). The paradigm shift toward multi-cores would require many longer global interconnects to communicate between cores, thus global wires would have to be pipelined deeper, in turn, latency becomes further worse. In this talk we examine the limits of Cu/low-κ interconnects and explore possible advantages of alternative technologies. The three most important novel potential candidates examined are optical and carbon nanotube (CNT)-based interconnects and three-dimensional (3-D) integration

Speaker Biography:

Prof. Krishna Saraswat is Rickey/Nielsen Professor in the School of Engineering, Professor of Electrical Engineering and Professor of Materials Science & Engineering (by courtesy) at Stanford University. He also has an honorary appointment of an Adjunct Professor at the Birla Institute of Technology and Science, Pilani, India since January 2004 and a D. J. Gandhi Chair Visiting Professor during the summer of 2007 at IIT Bombay, India. He serves as the Chair of Stanford's Materials Council and as the Associate Director of the NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing. He also serves on the leadership council of the MARCO Focus Center for Materials, Structures, and nano-Devices. His research interests are in new and innovative materials, structures, and process technology of silicon, germanium and III-V devices and interconnects for nanoelectronics. Prof. Saraswat has graduated more than 60 doctoral students and has authored or co-authored over 500 technical papers, of which six have received *Best Paper Award*. He is a Fellow of the IEEE, and a member of both The Electrochemical Society and The Materials Research Society.
He received a Ph.D. in Electrical Engineering from Stanford University in 1974.